AMENDMENT

In the Specification:

Please cancel the paragraphs at page 4, lines 2-7, and replace them with the following corrected paragraphs:

A1

Fig. 2 is a schematic cross-sectional view, taken along line 2-2 of Fig. 1, of a first embodiment of a scribe lane gettering plug on an SOI wafer, in accordance with the present invention.

Fig. 3 is a schematic cross-sectional view, taken along line 2-2 of Fig. 1, of a second embodiment of a scribe lane gettering plug on an SOI wafer, in accordance with the present invention.

Please cancel the paragraphs at page 6, lines 6-25, and replace them with the following corrected paragraphs:

A2

Fig. 2 shows a partial cross-sectional view of a portion of a gettering plug 108 taken along line 2-2 in Fig. 1. Fig. 2 shows a portion of the SOI wafer 100, including the silicon active layer 102, a buried oxide layer 110 and a silicon substrate 112. Fig. 2 indicates by vertical dashed lines an approximate area of a scribe lane 106. It will be recognized that the width of the scribe lane 106 may extend to the edge of the die pad 104. The SOI wafer 100 shown in Fig. 2 further includes a gettering plug 108. The gettering plug 108 may be separated from the silicon active layer 102, and thereby from the die pads 104 and the semiconductor devices thereon, by a sidewall liner 114. In Fig. 2, the gettering plug 108 extends through both the silicon active layer 102 and through the dielectric insulation layer 110 of the SOI wafer 100. In one embodiment, the SOI wafer 100 does not include a sidewall liner.